ABSTRACT

A system is disclosed in which an on-chip logic analyzer (OCLA) includes timestamp logic capable of providing clock cycle resolution of data entries using a relatively small number of bits. The timestamp logic includes a counter that is reset each time a store operation occurs. The counter counts the number of clock cycles since the previous store operation, and if enabled by the user, provides a binary signal to the memory that indicates the number of clock cycles since the previous store operation, which the memory stores with the state data. If the counter overflows before a store operation is requested, the timestamp logic may force a store operation so that the time between stores can be determined.